Amendment to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. – 17. (Canceled)

18. (Currently Amended) A stacked microelectronic device, comprising:

a first substrate ~~**of silicon, said substrate having a top surface**~~;

a plurality of interconnect structures formed on at least a portion of the **first** substrate;

a layer of ~~**material**~~ **polymer foam** formed on at least a portion of the ~~**top surface of the**~~ **first** substrate ~~**of silicon**~~ **adjacent to the interconnect structures, the polymer foam including polystyrene, polyester, polyurethane, or a combination thereof**; **and**

a second substrate ~~**of silicon**~~ with a plurality of interconnect structures formed thereon, said first and second substrate interconnect structures configured such that at least a portion of the interconnect structures of said first and second substrate respectively are in physical contact.

19. – 22. (Canceled)

23. (Previously Presented) The apparatus of claim 18, wherein the apparatus comprises a stacked chipset.

24. (Previously Presented) The apparatus of claim 18, wherein the first and second substrates comprise integrated circuits.

25. (Previously Presented) The apparatus of claim 18, wherein at least a portion of the interconnect structures comprise copper vias.

26.-29. (Canceled)

30. (New) A stacked microelectronic device, comprising:

a first substrate;

a plurality of interconnect structures formed on at least a portion of the first substrate;

a filler formed on at least a portion of the first substrate adjacent to the interconnect structures, the filler including a combination of

a first material including diisocyanate monomers, a diisocyanate end-capped compliant oligomer, p-toluenesulfonyl semicarbazide, or a combination thereof, and

a second material including water, a hydroxyl end-capped oligomer, a carboxylic acid end-capped polymer, or a combination thereof; and

a second substrate with a plurality of interconnect structures formed thereon, the first and second substrate interconnect structures configured such that at least a portion of the interconnect structures of the first and second substrate respectively are in physical contact.

31. (New) The apparatus of claim 30, wherein the apparatus comprises a stacked chipset.

32. (New) The apparatus of claim 30, wherein the first and second substrates comprise integrated circuits.

33. (New) The apparatus of claim 30, wherein at least a portion of the interconnect structures comprise copper vias.